

FEATURES

- ✓ Wide Operating Temperature Range
- ✓ Standard 5x7mm Package
- ✓ Rugged Hermetically Sealed Package
- ✓ Mil-Std-202 Compliant

Voltage Controlled Oscillator

#blileytakesyoufurther

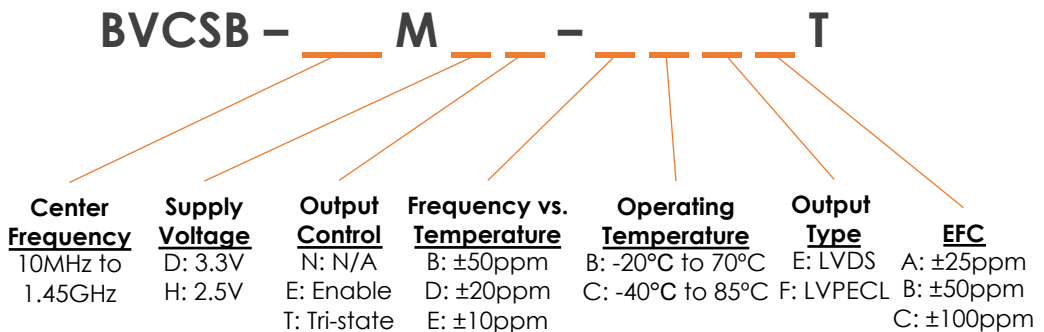
Description

Voltage Controlled Oscillators are designed to meet the rigorous demands of Military Standards as well as provide long life to OEM equipment manufacturers. Bliley Engineers Concurrent Design philosophy provides robust designs which are economical as well as reliable for long-term life. Applications consist of SATCOM, TELECOM, Military and Instrumentation.

Block Diagram



Part Number Configuration



*Not all combinations of options may be possible
 **Other options may be available

Performance Specifications

Parameter	Conditions	Values			Unit
		MIN	TYP	MAX	
Frequency Range		10M		1.45G	Hz
Initial Frequency Tolerance	Tested at +25°C			±1.5	ppm
Frequency Stability					
vs. Temperature	See Options (Max) Referenced to +25°C		±10, ±20, ±50		ppm
vs. Load	5% Change			±1	ppm
vs. Supply Voltage	5% Change			±1	ppm
Aging	1 Year			±2	ppm
Supply Voltage (Vdd)					
	Option D	3.13	3.3	3.47	Vdc
	Option E	4.75	5	5.25	Vdc
	Option H	2.37	2.5	2.63	Vdc
Current Consumption					
	10MHz			50	mA
	1.45GHz			150	mA
Output Control	Enabled Low Disabled High	30% Vdd		70% Vdd	
Electronic Frequency Control					
Voltage Range	@2.5V	0		2.5	Vdc
	@3.3V	0.15		3.15	Vdc
	@5V	0.5		4.5	Vdc
Center Voltage			Vdd/2		
Frequency Range	See Options (Min)		±25, ±50, ±100		ppm
Slope			positive		
Input Impedance			100		kΩ
Linearity			10		

Performance Specifications

Parameter	Conditions	Values			Unit
		MIN	TYP	MAX	
Output Characteristics (LVDS)		MIN	TYP	MAX	
High Output Level	Logic "1"		1.43		Vdc
Low Output Level	Logic "0"		1.10		Vdc
Rise/Fall Time				1	nSec
Duty Cycle		45	50	55	%
Load			100		Ω
Differential Output			330		mV
Offset Voltage			1.2		Vdc

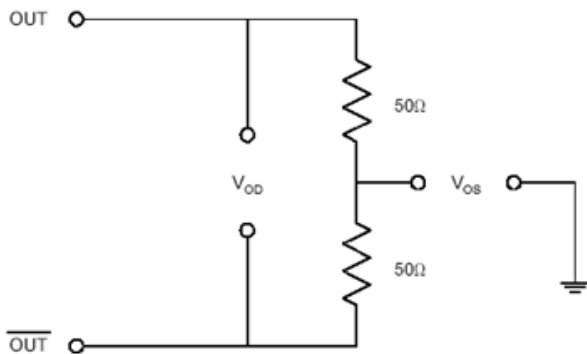
Parameter	Conditions	Values			Unit
		MIN	TYP	MAX	
Output Characteristics (PECL)		MIN	TYP	MAX	
High Output Level	Logic "1"	Vdd-1.025			Vdc
Low Output Level	Logic "0"			Vdd-1.62	Vdc
Rise/Fall Time				10	nSec
Duty Cycle		40	50	60	%
Load			50		Ω
High Output Level	Logic "1"	Vdd-1.025			Vdc
Low Output Level	Logic "0"			Vdd-1.62	Vdc

Performance Specifications

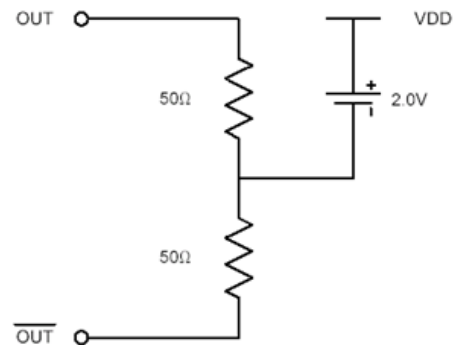
Parameter	Conditions	Values		Unit
		TYP	TYP	
Phase Noise		100MHz	125MHz	
Phase Noise (@ 25°C)	Offset			
	10Hz	-85	-80	dBc/Hz
	100Hz	-115	-110	dBc/Hz
	1kHz	-140	-135	dBc/Hz
	10kHz	-160	-145	dBc/Hz
	100kHz	-164	-155	dBc/Hz
	1MHz	-165	-165	dBc/Hz

Test Network

LVDS Levels Test Circuit



LVPECL Levels Test Circuit

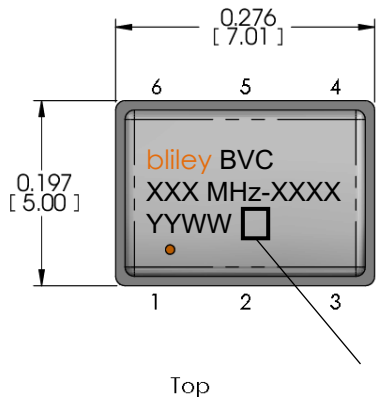


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Environmental Compliance

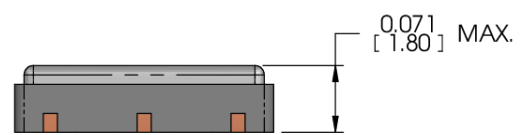
Parameter	Conditions	Values			Unit
		MIN	TYP	MAX	
Operating Temperature	Option B	-20		+70	°C
	Option C	-40		+85	°C
	Option D	-55		+125	°C
Storage Temperature		-55		+125	°C
Solderability	MIL-STD-202 Method 208				
Shock	MIL-STD-202 Method 213 Test Condition A				
Vibration	MIL-STD-202 Method 204 Test Condition C				

Physical Specifications

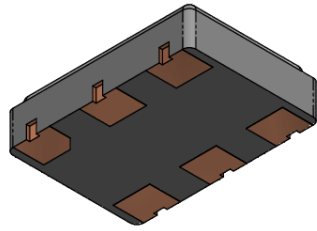


Top

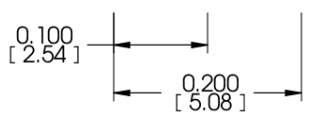
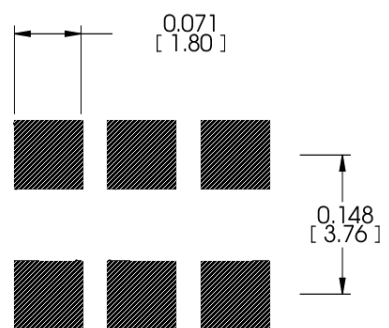
Traceability Code/SN



Side

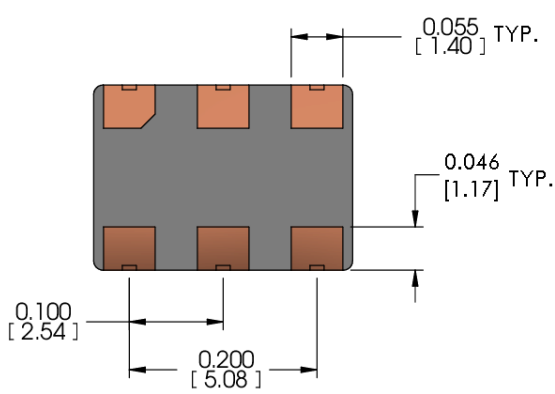


Iso Bottom



Recommended Landing Pattern

PIN	FUNCTION
1	EFC/N.C.
2	Output Control
3	Ground
4	RF Output
5	Complementary Output
6	Supply Voltage



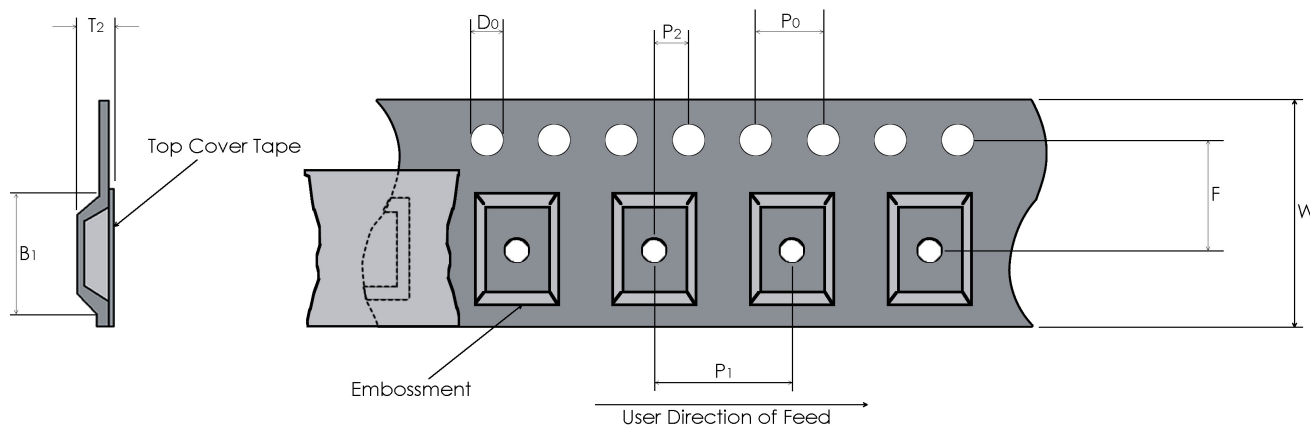
Bottom

Tolerances (mm) .X = ± 0.5, .XX = ±0.2 unless otherwise specified

Notes
1) None

Tape and Reel

Embossed Carrier Dimensions (8mm, 12mm, 16mm, 24mm Tape Only)



Tape Dimensions (mm)								Reel Dimensions (mm)	
W	F	Do	Po	P1	P2	B1	T2	Outside Dia.	Parts / Reel
16	7.5	1.5	4.0	8	2.0	7.6	2.4	180	1000

Recommended Reflow Profile

Reflow Profile: in accordance to IPC/JEDEC J-STD-020 (Latest Revision)

Additional Notes:

- This part has been designed for pick and place reflow soldering
- This part may be reflowed once
- This part should not be reflowed in the inverted position

Packaging

Packaging: All packaging must conform to ESD Controls detailed in ANSI/ESD S20.20 (Latest Revision)